Having thus described the aforementioned invention, we claim:

1. An apparatus for transferring multiplexed multiple multi-bit messages across a bit level network, said apparatus comprising:

a network interface for accessing the bit level network, said network interface configured to transmit and receive a message at a preselected one of a plurality of time-division multiplex addresses on each channel of a preselected channel set;

a processor in communication with said network interface;

a memory in communication with said processor; and

a second interface for connecting either an input or an output device to said processor;

whereby the multiple multi-bit messages are transmitted over said network interface.

2. The apparatus of Claim 1 wherein said network interface includes a clock signal and a data signal.

3. The apparatus of Claim 2 wherein said data signal is a serial data stream synchronized with the said clock signal.

4. The apparatus of Claim 2 wherein said data signal includes said message, said message including a command segment and a data segment, said command segment includes at least an operator and an operand.

5. The apparatus of Claim 4 wherein said command segment is a serial bitstream starting at a specified address determined by said clock signal on a first channel of said preselected channel set and said data segment is a serial bitstream starting at said specified address on a second channel of said preselected channel set.

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1          6. The apparatus of Claim 4 wherein said operator includes a read
request, said memory at a location specified by said operand contains data which
is copied to said data segment.

1          7. The apparatus of Claim 4 wherein said operator includes a write
request, said data segment contains data which is copied to said memory at a
location specified by said operand.

1          8. A method for transferring large amounts of complex data between a
data link module and a host across a bit level network , said method comprising
the steps of:
          (a) configuring a channel set to said data link module;
5          (b) configuring a frame address to said data link module;
          (c) sending a message from said host to said data link module, said
message including a message command segment on a first channel of said channel
set at said data link module frame address and a message data segment on a
second channel of said channel set at said data link module frame address, said
10        message command segment including a register operand and at least either of a
read request or a write request;
          (d) accessing a register in said data link module specified in said register
operand as a specified register;
          (e) sending a reply from said data link module to said host, said reply
15        including a reply command segment on a first channel of said channel number pair
at said data link module frame address and a reply data segment on a second
channel of said channel number pair at said data link module frame address.

1          9. The method of Claim 8 wherein said message command segment
includes a read request, said step of accessing a register in said data link module
further comprises the step of reading a value from said specified register as a read
value.

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1        10. The method of Claim 9 wherein said reply command segment equals said message command segment and said reply data segment contains said read value.

1        11. The method of Claim 8 wherein said message command segment includes a write request, said step of accessing a register in said data link module further comprises the step of writing said message data segment to said specified register.

1        12. The method of Claim 11 wherein said reply command segment equals said message command segment and said reply data segment equals said message data segment.

1        13. A data link module connected to a data bus and a master clock line for use in a bit level network system having multiple data link modules, the master clock line for generating a predetermined number of time slots for a complete multiplexed channel, each time slot on the complete multiplexed channel

5        associated with an address location of at least one data link module or a data bit on the data bus, said data link module comprising:

        means for interfacing with either an input device or an output device;

        means for receiving data from the data bus at a predetermined time slot on a first multiplexed channel, said data being a multiplexed multibit message

10       including at least a command segment and a data segment;

        means for sending data to the data bus during said predetermined time slot on a second multiplexed channel;

        means for processing said data;

        means for storing said data; and

15       means for retrieving said data.